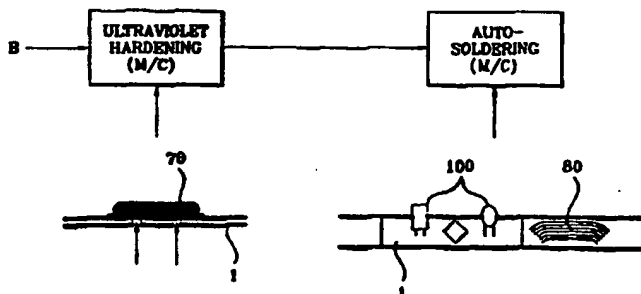




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H05K 3/30, C09J 5/00	A1	(11) International Publication Number: WO 95/09521 (43) International Publication Date: 6 April 1995 (06.04.95)
(21) International Application Number: PCT/KR94/00127 (22) International Filing Date: 22 September 1994 (22.09.94) (30) Priority Data: 1993/19264 22 September 1993 (22.09.93) KR (71) Applicant (for all designated States except US): SAMSUNG ELECTRONICS CO., LTD. [KR/KR]; 413, Maetan-dong, Paldal-gu, Suwon-city, Kyungki-do 441-370 (KR). (72) Inventor; and (75) Inventor/Applicant (for US only): KIM, Sang, Ju [KR/KR]; Samsung Electronics Co., Ltd., 413, Maetan-dong, Paldal-gu, Suwon City, Kyungki-do 441-370 (KR). (74) Agent: CHO, Yong, Shik; 264-298, Imun 2-dong, Tongdaemun-gu, Seoul 130-082 (KR).		(81) Designated States: JP, RU, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: LOCAL HARDENING METHOD OF A SEMICONDUCTOR INTEGRATED CIRCUIT**(57) Abstract**

The local hardening method of a semiconductor integrated circuit is carried out through the steps of forming a hardening hole on a semiconductor integrated circuit at its attachment place with the PCB wafer for auto-inserting, detecting defects, reversing PCB to show an upper copper-clad side of the PCB, and coating a designated hole point of the reversed PCB with bond in a local bonding machine, so that the semiconductor integrated circuit can be mounted precisely on a designated point by coordinates in a semiconductor local mounting machine, by regulating soldering shapes by an auto-soldering machine after a semiconductor integrated circuit is attached, by passing ultraviolet rays through the hardening hold in an ultraviolet hardening machine and attaching and fixing a semiconductor integrated circuit on the copper-clad side of the PCB, so that the improvement of the productivity can be achieved by clearing up mounting twist, cooling solder, soldering short, and coming off phenomena of the attached semiconductor integrated circuit and making auto-mounting and auto-soldering of the semiconductor integrated circuit possible.

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LOCAL HARDENING METHOD OF A SEMICONDUCTOR INTEGRATED CIRCUIT

Technical Field

This invention relates to a local mounting and hardening method of a semiconductor, for a example to mount and harden a Quad Flat Package integrated circuit locally by using a hole formed in PCB(Printed Circuit Board). More particularly, it relates to a local hardening method of a semiconductor integrated circuit in which a conventional manual soldering method is converted to an automatic soldering method by making local mount of a semiconductor integrated circuit on a PCB assembly frame possible.

Background Art

According to a conventional method, as shown in FIG.1A to FIG.1D, in SMT(System Multi Tester) mounting process, an mounting-impossible point of an integrated circuit 10 is manually put on PCB, a lead and PCB solder land 15 are united and fixed by pressing the integrated circuit by hands, and every lead 20 is manually soldered in every direction by a soldering iron.

The conventional soldering method is described more concretely with reference to FIGS. 1A-1D.

As shown in FIG.1A, a semiconductor integrated circuit is attached on a PCB wafer after fitting it in its mounting direction, and the locations of a lead 20 and a solder land 15 are

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manually adjusted and set up. As shown in FIG.1B, the upper circuit 10 is lightly pressed and held by left fingers. The lead 20 of the circuit 10 is coated with flux with a brush. Generally, said flux is coated in the directions of A side and B side (lengthwise and widthwise). When said process is finished, as shown in FIG.1C, an iron 30 covered with a small amount of solder moves following the arrow and solder the part A of FIG.1B. It also moves to parts B, C, and D to solder them in the same method.

When the solder is finished, cooling and contact of the solder are inspected by a microscope 33. If contacted, the soldering iron 30 is moved to the lead 20 direction, as it were, to the outside direction (E direction of FIG.1D) and removed.

The above-mentioned conventional manual mounting and soldering method has disadvantages to need much time and a worker's long time attention in order to prevent mounting twist to be generated by the reason that the semiconductor integrated circuit fails to land precisely on the PCB in the range of 0.3mm to 0.4mm. Cooling solder and soldering short phenomenon is also much generated, the long time for inspection is required, and degradation of the quality is happened.

Disclosure of Invention

This invention has purposes to prevent mounting twist, cooling solder, soldering short, and coming off of a semiconductor integrated circuit and to provide a local hardening method of a semiconductor integrated circuit which makes automatic soldering possible and improves quality and reliability of goods by making a

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0.8mm x 3.0mm's cross-shaped hole on a semiconductor integrated circuit to safely attach to the PCB wafer, coating the hole with bond automatically, mounting the semiconductor integrated circuit by coordinates automatically, and hardening locally by ultraviolet rays through the cross-shaped hole.

To achieve said purposes, a local hardening method of a semiconductor integrated circuit of this invention has characteristics to be comprised of the steps of forming a hardening hole on a semiconductor integrated circuit at its attachment place with the PCB wafer for auto-inserting, detecting whether any defect exists in the auto-inserted parts of PCB box in APTs(Auto Program Testers), reversing PCB in a PCB reverser so as to show an upper copper-clad side of the PCB, coating a designated hole point of the reversed PCB with bond in a local bonding machine, mounting precisely the semiconductor integrated circuit on a designated point by coordinates in a semiconductor local mounting machine, and regulating soldering shapes by an auto-soldering machine after a semiconductor integrated circuit is attached, by passing ultraviolet rays through the hardening hole in an ultraviolet hardening machine and attaching and fixing a semiconductor integrated circuit on the copper-clad side of the PCB.

Brief Description of Drawings

FIG.1A to FIG.1D are schematic diagrams to show mounting and soldering process of a conventional semiconductor integrated circuit.

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FIG.2A and FIG.2B are diagrams to show hardening holes of a semiconductor integrated circuit according to this invention.

FIG.3 to FIG.3C are schematical diagrams to show a local hardening method of a semiconductor integrated circuit according to this invention.

Best Mode for Carrying Out the Invention

A preferred embodiment of a local hardening method of a semiconductor integrated circuit in accordance with this invention is explained in detail with appended diagrams hereinafter.

FIG.3A to FIG.3C are block diagrams to briefly show a local hardening method of a semiconductor integrated circuit according to this invention. First of all, a hardening hole 50 in the shape of "+", as shown in FIG.2A and FIG.2B, is formed on a semiconductor integrated circuit at its attachment place with a PCB, and auto-inserting is carried out. Though the cross shape ("+") is desirable for the hardening hole, such polygonal shapes like a circle, square, and triangle are also possible if necessary. The number of hardening holes is at least one. Though five hardening holes in the shape of "+" may be set up in the various directions in FIG. 2A and FIG. 2B, it is desirable to set them up in mainly diagonal direction. Preferably, interval of the hole shown in FIG. 2A is to be under 20mm and hole size is 0.7mm x 1.5mm to 1.0mm x 5.0mm.

After detecting any existence of defect in the auto-inserted parts of auto-inserted PCB box in the APT(Auto Program Tester), if any defect is not exist, the PCB wafer 1 is

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reverted by the PCB reverser to show a copper-clad side, the upper side thereof. Reference symbol M/C indicates a machine in the drawings and reference symbol 100 represents each accessory part.

5 The points 60 of designated hardening hole of the reversed PCB wafer 1 are coated with bond in a semiconductor local bonding machine. A surrounding pattern of the hardening hole on the PCB is set up and can be removed, so coming off phenomenon of the attached semiconductor integrated circuit can be prevented while mounting the semiconductor.

10 In a semiconductor local mounting machine, mounting is performed by coordinates to precisely mount a semiconductor integrated circuit on the designated point. After the semiconductor integrated circuit is mounted, ultraviolet rays are passed to the arrow direction through the hardening hole 50 in the
15 ultraviolet-ray hardening machine and a semiconductor integrated circuit 70 is attached and fixed on the copper-clad side 40 of the PCB, and then soldering shape is regulated the auto soldering machine and finished. Unexplained reference symbol 80 is soldering bath.

20 According to the invention, the semiconductor can be attached to the PCB by less workers, reducing the regradation in the quality and achieve the improvement of the productivity by clearing up mounting twist, cooling solder, soldering short, and coming off phenomena of the attached semiconductor integrated
25 circuit and making auto-mounting and auto-soldering of the semiconductor integrated circuit possible.

While the present invention has been particularly shown and described with reference to a particular embodiment thereof,

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it will be understood by those skilled in the art that various changes in form and details may be effected therein without departing from the spirit and scope of the invention as defined by the appended claims.

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CLAIMS

1. A local hardening method of a semiconductor integrated circuit, comprising the steps of

forming a hardening hole on a semiconductor integrated circuit at its attachment place with the PCB wafer for
5 auto-inserting,

detecting whether any defect exists in the auto-inserted parts of PCB box in APTs(Auto Program Testers),

reversing PCB in a PCB reverser so as to show an upper copper-clad side of the PCB,

10 coating a designated hole point of the reversed PCB with bond in a local bonding machine,

mounting precisely the semiconductor integrated circuit on a designated point by coordinates in a semiconductor local mounting machine, and

15 regulating soldering shapes by an auto-soldering machine after a semiconductor integrated circuit is attached, by passing ultraviolet rays through the hardening hole in an ultraviolet hardening machine and attaching and fixing a semiconductor integrated circuit on the copper-clad side of the PCB.

20 2. The method according to claim 1, wherein said hardening hole is formed in the shape of a circle.

3. The method according to claim 1, wherein said hardening hole is formed in the shape of a triangle. 0.

4. The method according to claim 1, wherein said

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hardening hole is formed in the shape of a square.

5. The method according to claim 1, said hardening hole is formed in the shape of a polygon.

6. The method according to claim 1, said hardening hole
5 number is one.

7. The method according to claim 1, wherein said hardening hole number is two to five.

8. The method according to claim 1, wherein said hardening holes formed in the pitch under 20mm.

10 9. The method according to claim 1, wherein a surrounding pattern around said PCB holes are removable to prevent coming off phenomenon of the attached semiconductor integrated circuit while mounting the semiconductor integrated circuit.

10. The method according to claim 1, wherein said
15 hardening holes are formed in the size of 0.7mm x 1.5mm to 1.0mm x 5.0mm.

FIG. 1
PRIOR ART

FIG. 1A

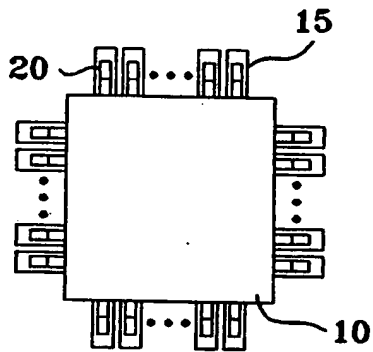


FIG. 1B

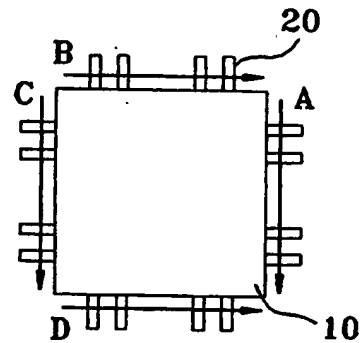


FIG. 1C

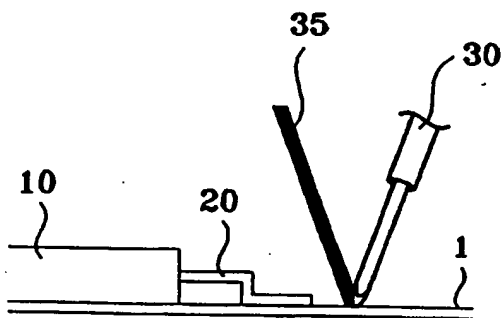
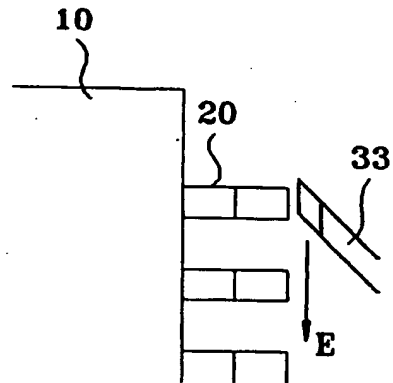


FIG. 1D



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FIG.2A

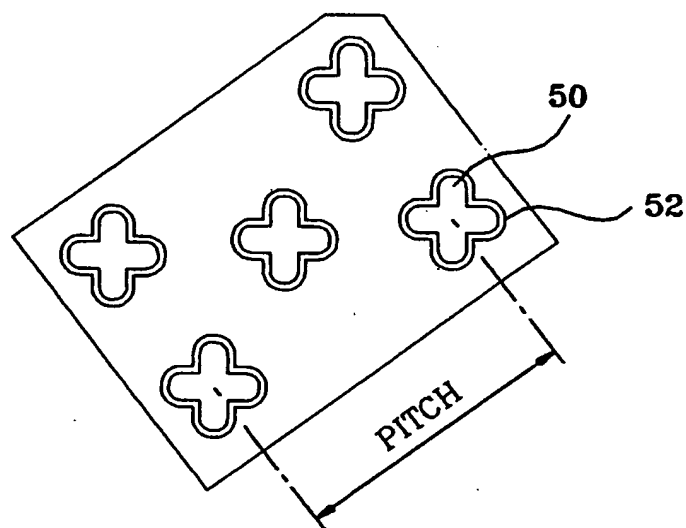


FIG.2B

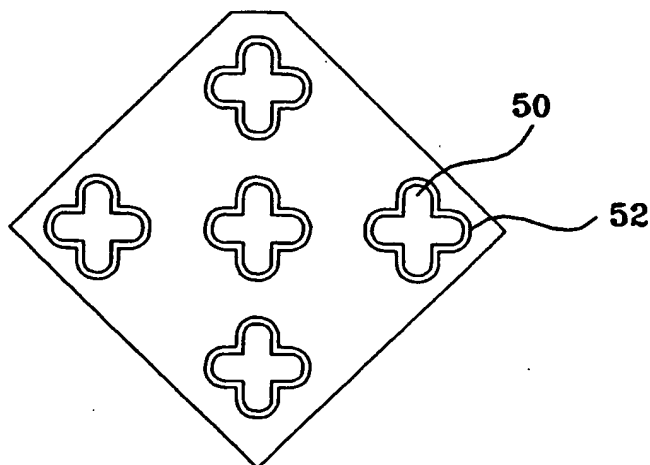
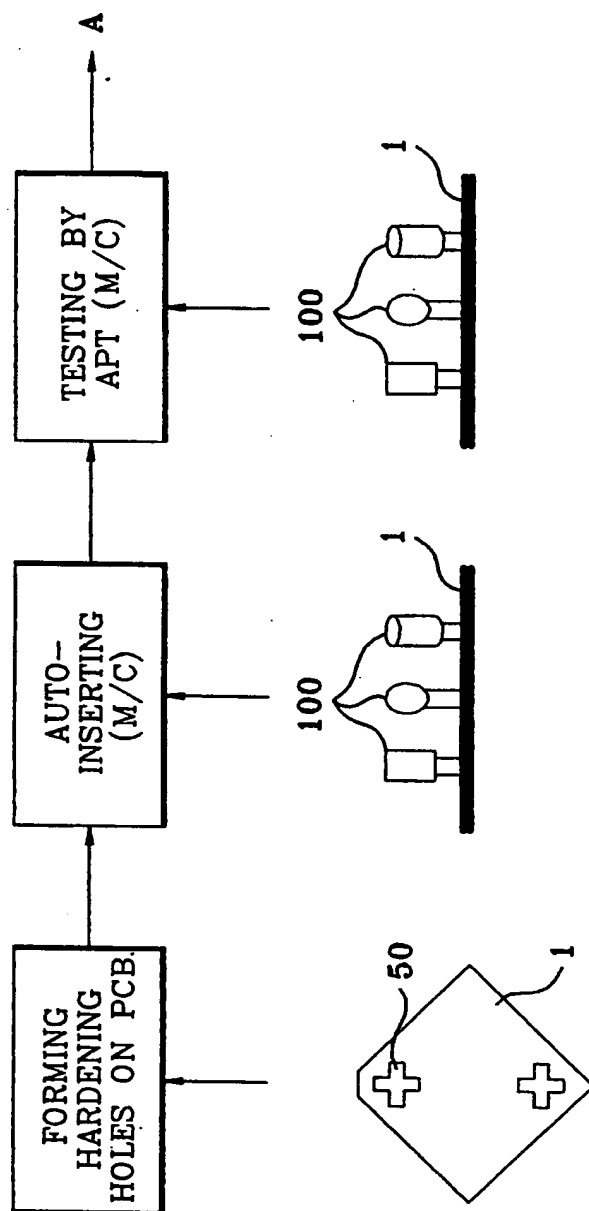


FIG.3A



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FIG. 3B

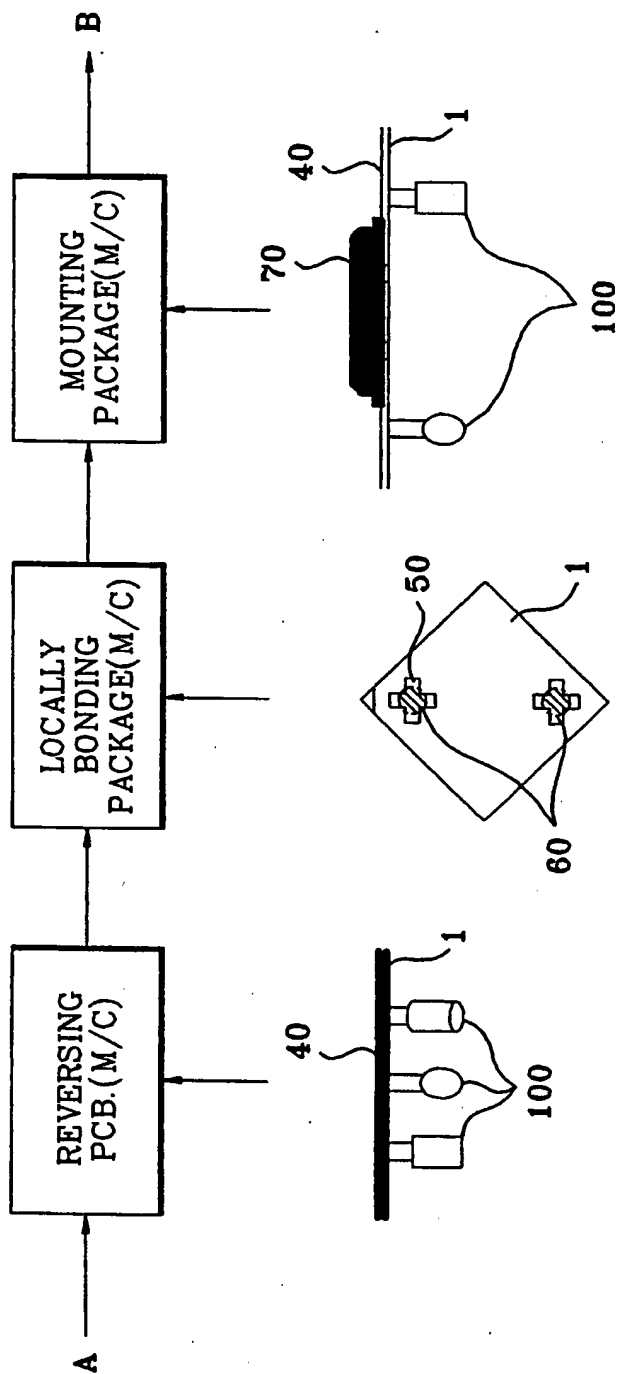
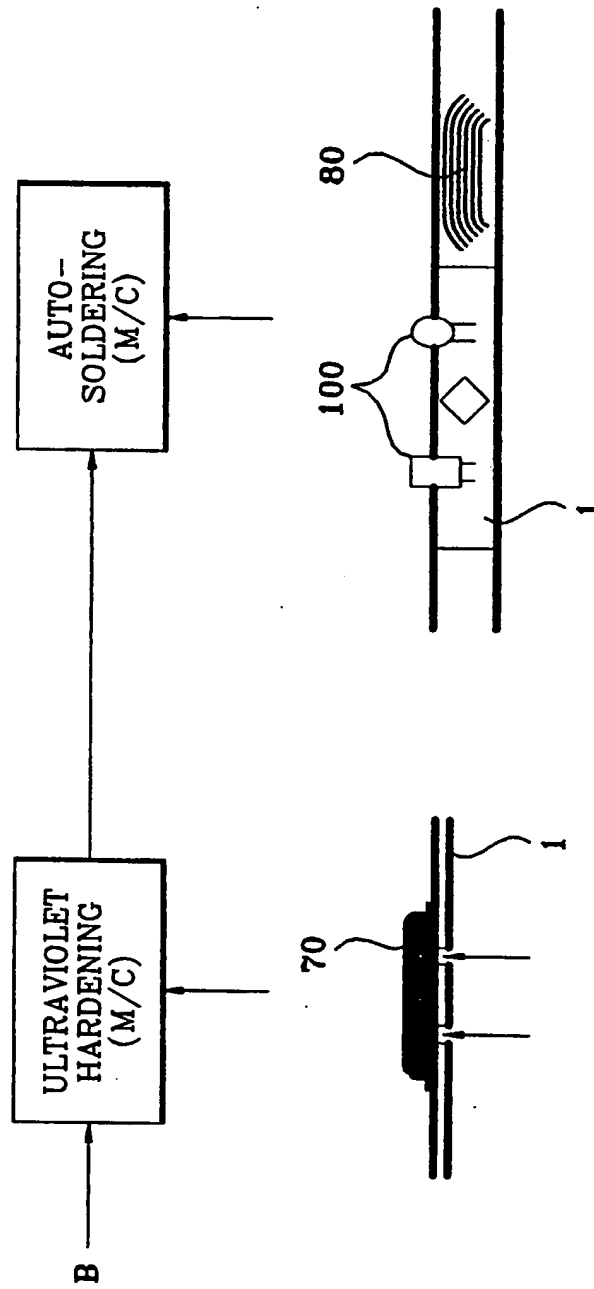


FIG. 3C



INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR 94/00127

A. CLASSIFICATION OF SUBJECT MATTER

IPC⁶: H 05 K 3/30, C 09 J 5/00

According to International Patent Classification (IPC) or to both national classification and IPC

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP, A, 0 378 233 (MATSUSHITA ELECTRIC INDUSTRIAL) 18 July 1990 (18.07.90), claims 1,5.	1
A	EP, A, 0 330 909 (ESPE STIFTUNG) 06 September 1989 (06.09.89), abstract.	1
A	EP, A, 0 218 832 (SIEMENS AKTIENGESSELLSCHAFT) 22 April 1987 (22.04.87), abstract, fig. 2.	1
A	EP, A, 0 016 984 (MATSUSHITA ELECTRIC INDUSTRIAL) 15 October 1980 (15.10.80), abstract, fig. 6.	1

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

12 January 1995 (12.01.95)

Date of mailing of the international search report

31 January 1995 (31.01.95)

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			EP B1	378233	28-12-94
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